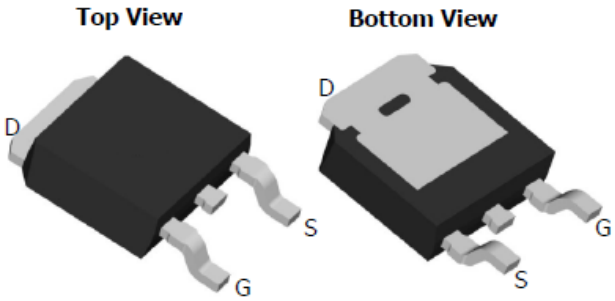
650V N-Channel Enhancement Mode MOSFET

RoHS COMPLIANT

Description

The XPX7N65RD is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.



General Features

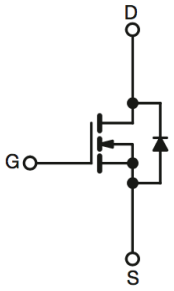
V_{DS} = 650V I_D =7A

$R_{DS(ON)}$ < 1.2Ω @ V_{GS}=10V （Type： 1.0Ω）

Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



N-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
XPX7N65RD	TO-252-3L	XPX7N65RD XXX YYYY	2500
XPX7N65RD	TO-251-3L	XPX7N65RD XXX YYY	4000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Value	Unit
		TO-252 TO-251	
VDSS	Drain-Source Voltage (V_{GS} = 0V)	650	V
ID	Continuous Drain Current	7	A
IDM	Pulsed Drain Current (note1)	28	A
VGS	Gate-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy (note2)	247	mJ
IAR	Avalanche Current (note1)	7	A
E_{AR}	Repetitive Avalanche Energy note1)	18	mJ
P_D	Power Dissipation (T_C = 25ºC)	32.9	W
TJ, Tstg	Operating Junction and Storage Temperature Range	-55~+150	ºC
RthJC	Thermal Resistance, Junction-to-Case	3.8	ºC/W
RthJA	Thermal Resistance, Junction-to-Ambient	13.3	ºC/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	650	685	--	V
IDSS	Zero Gate Voltage Drain Current	V_{DS}= 650V, V_{GS}= 0V, T_J=25ºC	--	--	1	μA
IGSS	Gate-Source Leakage	V_{GS} = ±30V	--	--	±100	nA
VGS(th)	Gate-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	2.0	--	4.0	V
RDS(on)	Drain-Source On-Resistance (Note3)	V_{GS} = 10V, I_D = 3.5A	--	1.0	1.2	Ω
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz	--	1000	--	pF
C_{oss}	Output Capacitance		--	101	--	
C_{rss}	Reverse Transfer Capacitance		--	1.5	--	
Q_g	Total Gate Charge	V_{DD}=520V, I_D = 7A, V_{GS} = 10V	--	22	--	nC
Q_{gs}	Gate-Source Charge		--	4.3	--	
Q_{gd}	Gate-Drain Charge		--	13	--	
td(on)	Turn-on Delay Time	V_{DD}=325V, I_D = 7A, R_G = 25Ω	--	12	--	ns
t_r	Turn-on Rise Time		--	26	--	
td(off)	Turn-off Delay Time		--	29	--	
t_f	Turn-off Fall Time		--	27	--	
IS	Continuous Body Diode Current	T_C = 25 ºC	--	--	7.0	A
ISM	Pulsed Diode Forward Current		--	--	28	A
V_{SD}	Body Diode Voltage	T_J = 25ºC, I_{SD} = 7A, V_{GS} = 0V	--	--	1.4	V
trr	Reverse Recovery Time	V_{GS} = 0V,I_S = 7A, di_F/dt =100A /μs	--	389	--	ns
Q_{rr}	Reverse Recovery Charge		--	2.04	--	μC

Note :

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The EAS data shows Max. rating . IAS = 4.5A, VDD = 50V, RG = 25 Ω, Starting TJ = 25 ºC

3、The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

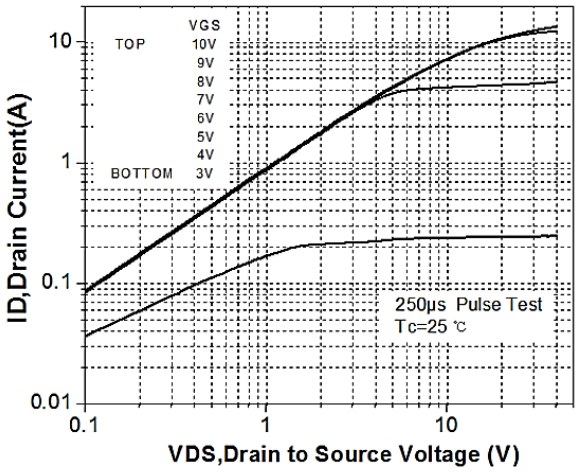


Figure 1. On-Region Characteristics

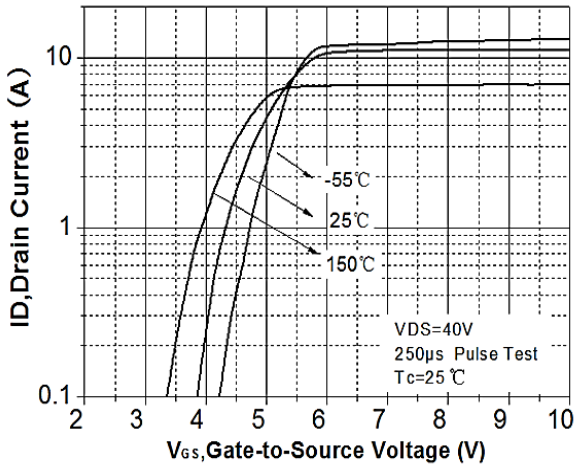


Figure 2. Transfer Characteristics

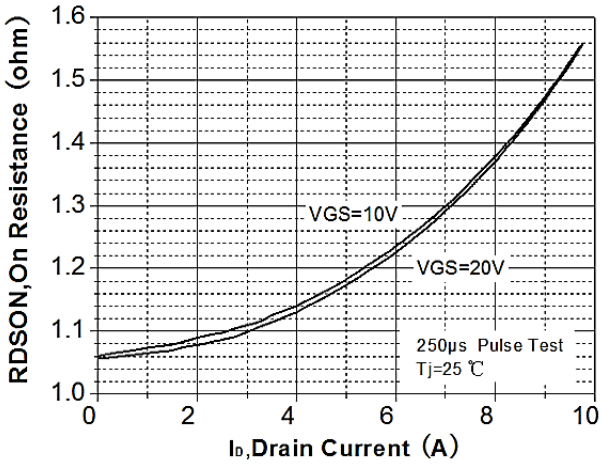


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

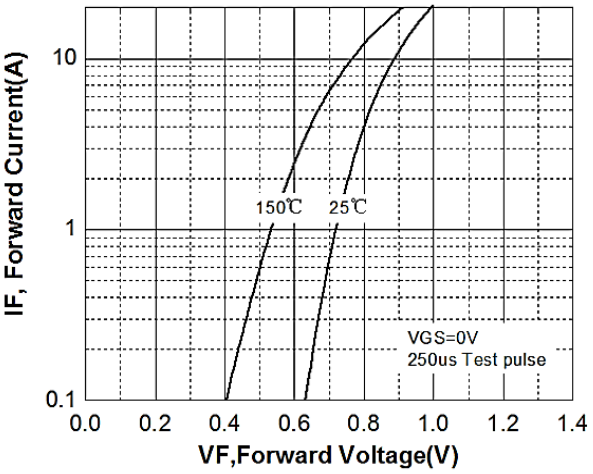


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

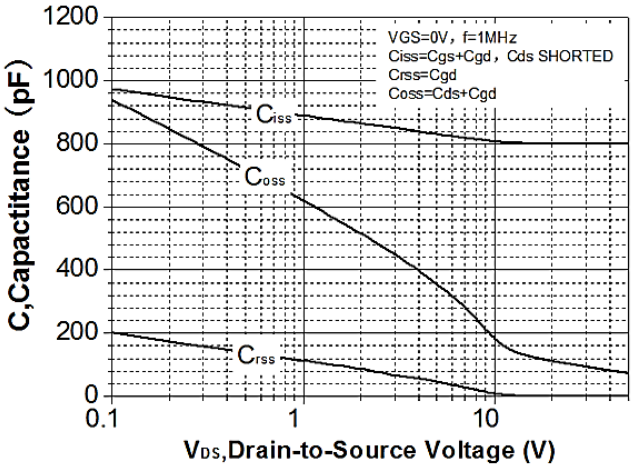


Figure 5. Capacitance Characteristics

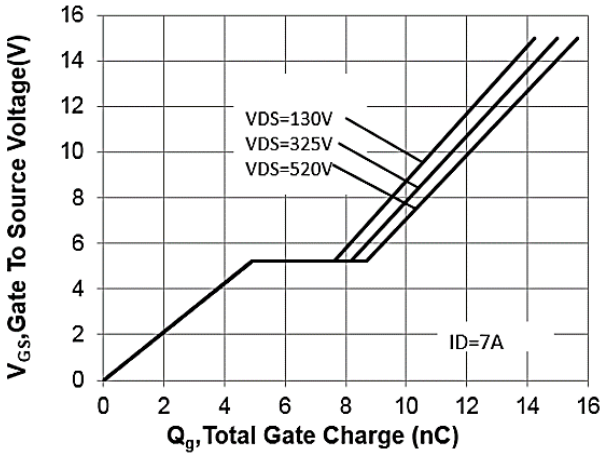
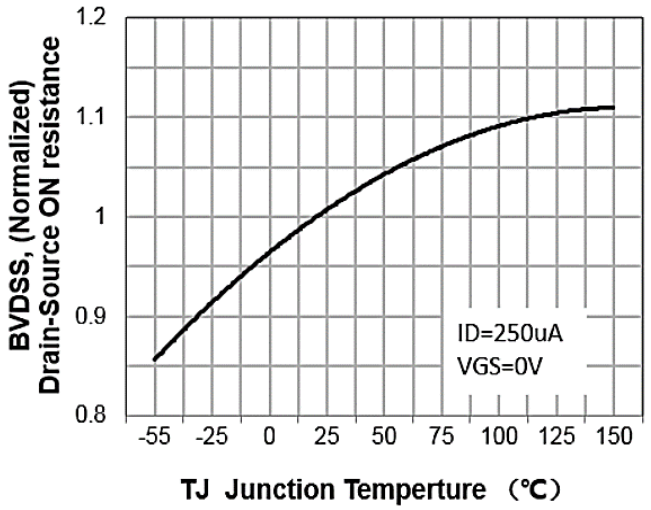


Figure 6. Gate Charge Characteristics



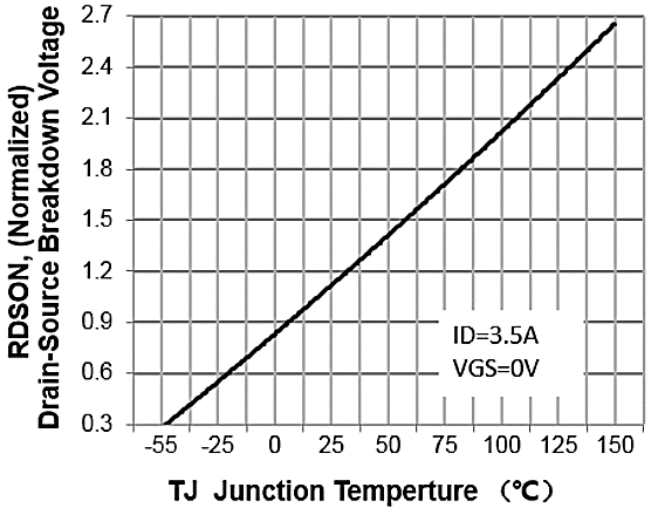
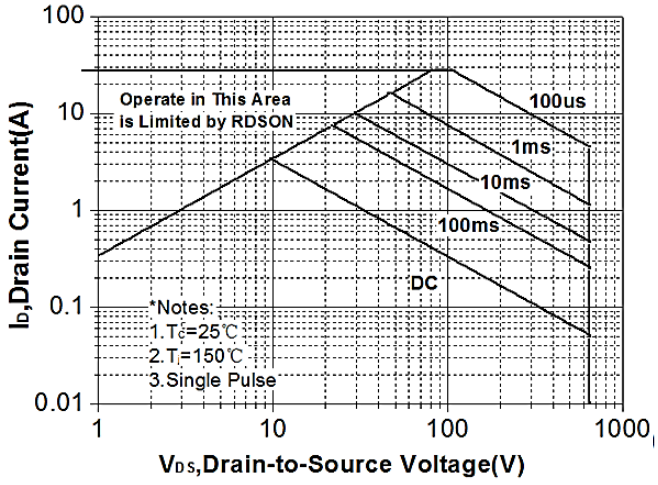


Figure 7. Breakdown Voltage Variation vs Temperature

Figure 8. On-Resistance Variation vs Temperature



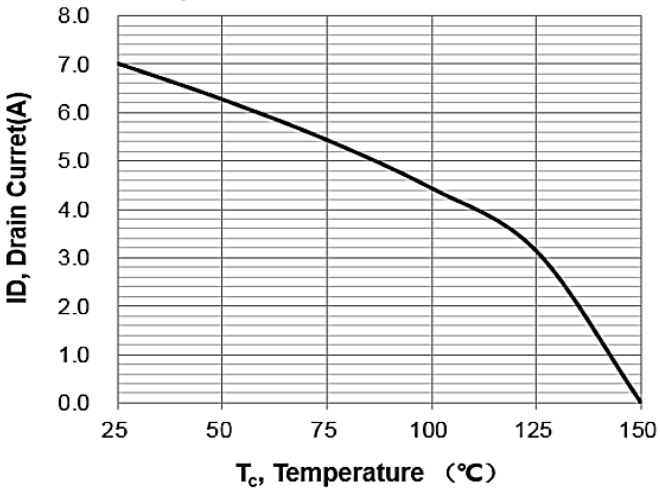


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs Case Temperature

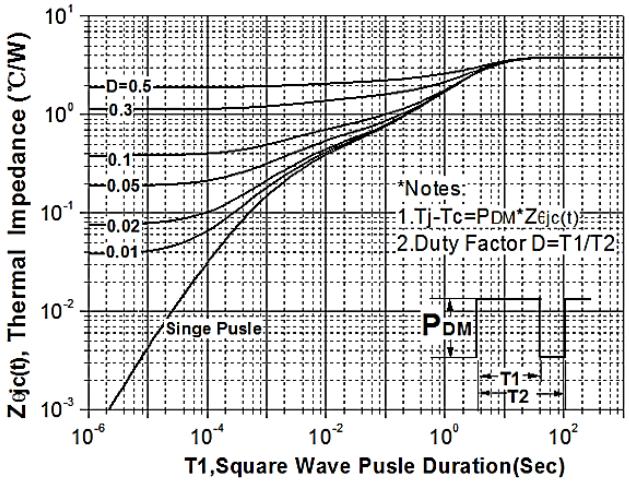


Figure 11. Transient Thermal Response Curve

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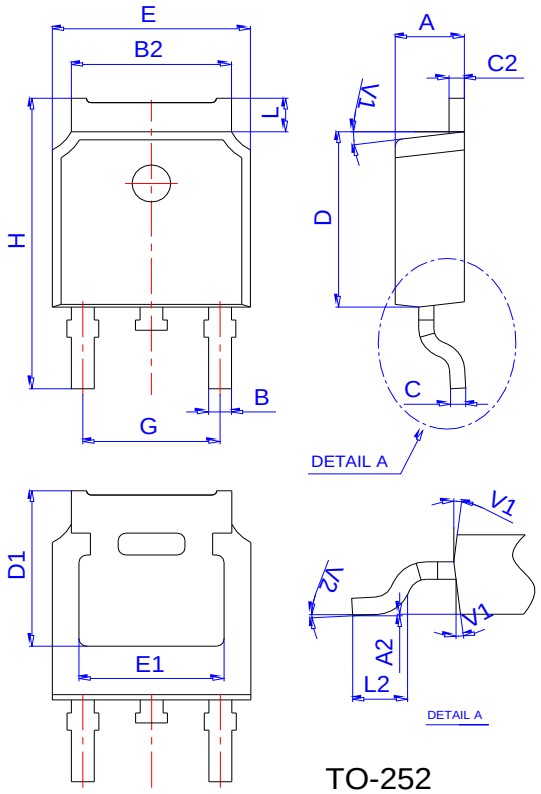
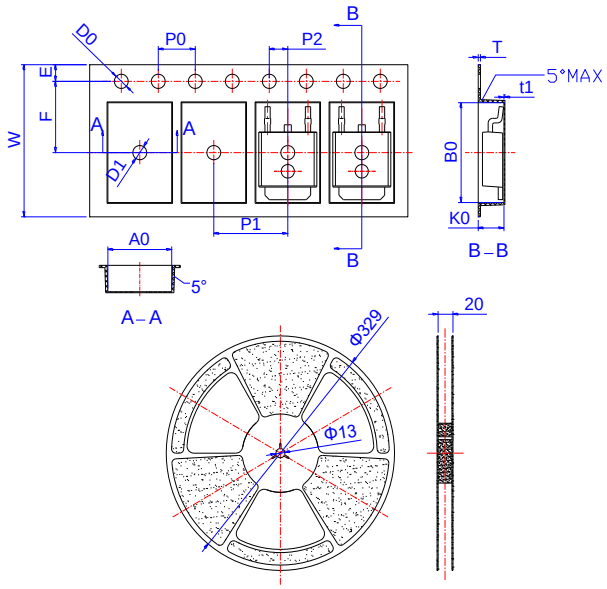
Package Mechanical Data



TO-252

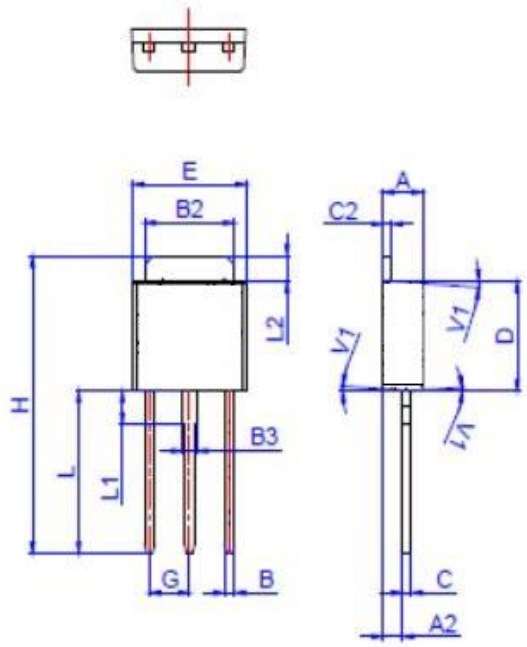
Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

Package Mechanical Data



TO-251

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.20		2.40	0.086		0.095
A2	0.90		1.20	0.035		0.047
B	0.55		0.65	0.022		0.026
B2	5.10		5.40	0.200		0.213
B3	0.76		0.85	0.030		0.033
C	0.45		0.62	0.018		0.024
C2	0.48		0.62	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.70	0.252		0.264
G		2.30			0.091	
H	16.0		17.0	0.630		0.669
L	8.90		9.40	0.350		0.370
L1	1.80		1.90	0.071		0.075
L2	1.37		1.50	0.054		0.059
V1		4°			4°	

Package Information -TO-251

OUTLINE	TUBE (PCS)	INNER BOX (PCS)	PER CARTON (PCS)
TUBE	80	4,000	32,000

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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