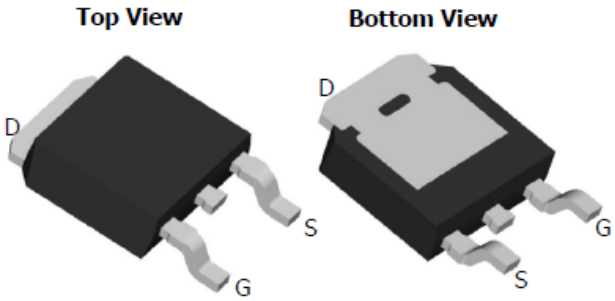
# XPX60N04D

## 40V N-Channel Enhancement Mode MOSFET

### Description

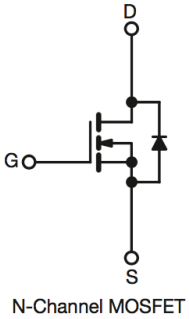
The XPX60N04D uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.




### General Features

$V_{DS}$ = 40V $I_D$ =60 A

$R_{DS(ON)}$ < 18.5mΩ @ $V_{GS}$=10V



N-Channel MOSFET

### Application

Battery protection

Load switch

Uninterruptible power supply

### Package Marking and Ordering Information

| Product ID | Pack | Marking | Qty(PCS) |
|---|---|---|---|
| XPX60N04D | TO-252-3L | XPX60N04D XXX YYYY | 2500 |

### Absolute Maximum Ratings ($T_C$=25℃unless otherwise noted)

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| $V_{DS}$ | Drain-Source Voltage | 40 | V |
| $V_{GS}$ | Gate-Source Voltage | ±20 | V |
| $I_D$@$T_C$=25℃ | Continuous Drain Current, $V_{GS}$ @ 10V[1] | 60 | A |
| $I_D$@$T_C$=100℃ | Continuous Drain Current, $V_{GS}$ @ 10V[1] | 26 | A |
| $I_D$@$T_A$=25℃ | Continuous Drain Current, $V_{GS}$ @ 10V[1] | 10 | A |
| $I_D$@$T_A$=70℃ | Continuous Drain Current, $V_{GS}$ @ 10V[1] | 8 | A |
| $I_{DM}$ | Pulsed Drain Current[2] | 100 | A |
| EAS | Single Pulse Avalanche Energy[3] | 31 | mJ |
| $I_{AS}$ | Avalanche Current | 25 | A |
| $P_D$@$T_C$=25℃ | Total Power Dissipation[4] | 34.7 | W |
| $P_D$@$T_A$=25℃ | Total Power Dissipation[4] | 2 | W |
| $T_{STG}$ | Storage Temperature Range | -55 to 150 | ℃ |
| $T_J$ | Operating Junction Temperature Range | -55 to 150 | ℃ |
| $R_{\theta JA}$ | Thermal Resistance Junction-ambient (Steady State)[1] | 62 | ℃/W |
| $R_{\theta JC}$ | Thermal Resistance Junction-Case[1] | 3.6 | ℃/W |

## Electrical Characteristics ($T_J$=25 ℃, unless otherwise noted)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V , $I_D$=250uA | 40 | --- | --- | V |
| $\triangle BV_{DSS}/\triangle T_J$ | BVDSS Temperature Coefficient | Reference to 25℃ , $I_D$=1mA | --- | 0.034 | --- | V/℃ |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance[2] | $V_{GS}$=10V , $I_D$=20A | --- | 14.5 | 18.5 | mΩ |
| | | $V_{GS}$=4.5V , $I_D$=10A | --- | 17.5 | 20.5 | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{GS}$=$V_{DS}$ , $I_D$ =250uA | 1.0 | 1.5 | 2.5 | V |
| $\triangle V_{GS(th)}$ | $V_{GS(th)}$ Temperature Coefficient | | --- | -5.64 | --- | mV/℃ |
| $I_{DSS}$ | Drain-Source Leakage Current | $V_{DS}$=32V , $V_{GS}$=0V , $T_J$=25℃ | --- | --- | 1 | uA |
| | | $V_{DS}$=32V , $V_{GS}$=0V , $T_J$=55℃ | --- | --- | 5 | |
| $I_{GSS}$ | Gate-Source Leakage Current | $V_{GS}$=±20V , $V_{DS}$=0V | --- | --- | ±100 | nA |
| gfs | Forward Transconductance | $V_{DS}$=5V , $I_D$=20A | --- | 36 | --- | S |
| $R_g$ | Gate Resistance | $V_{DS}$=0V , $V_{GS}$=0V , f=1MHz | --- | 2.1 | 4.2 | Ω |
| $Q_g$ | Total Gate Charge (4.5V) | $V_{DS}$=20V , $V_{GS}$=4.5V , $I_D$=12A | --- | 10.7 | --- | nC |
| $Q_{gs}$ | Gate-Source Charge | | --- | 3.3 | --- | |
| $Q_{gd}$ | Gate-Drain Charge | | --- | 4.2 | --- | |
| $T_{d(on)}$ | Turn-On Delay Time | $V_{DD}$=12V , $V_{GS}$=10V , $R_G$=3.3 $I_D$=6A | --- | 8.6 | --- | ns |
| $T_r$ | Rise Time | | --- | 3.4 | --- | |
| $T_{d(off)}$ | Turn-Off Delay Time | | --- | 25 | --- | |
| $T_f$ | Fall Time | | --- | 2.2 | --- | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$=15V , $V_{GS}$=0V , f=1MHz | --- | 1314 | --- | pF |
| $C_{oss}$ | Output Capacitance | | --- | 120 | --- | |
| $C_{rss}$ | Reverse Transfer Capacitance | | --- | 88 | --- | |
| $I_S$ | Continuous Source Current[1,5] | $V_G$=$V_D$=0V , Force Current | --- | --- | 42 | A |
| $I_{SM}$ | Pulsed Source Current[2,5] | | --- | --- | 100 | A |
| $V_{SD}$ | Diode Forward Voltage[2] | $V_{GS}$=0V , $I_S$=1A , $T_J$=25℃ | --- | --- | 1.2 | V |

Note :

1.The data tested by surface mounted on a 1 inch$^2$ FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3.The EAS data shows Max. rating . The test condition is $V_{DD}$=25V,$V_{GS}$=10V,L=0.1mH,$I_{AS}$=25A

4.The power dissipation is limited by 150℃ junction temperature

5 .The data is theoretically the same as $I_D$ and $I_{DM}$ , in real applications , should be limited by total power dissipation.

## Typical Characteristics

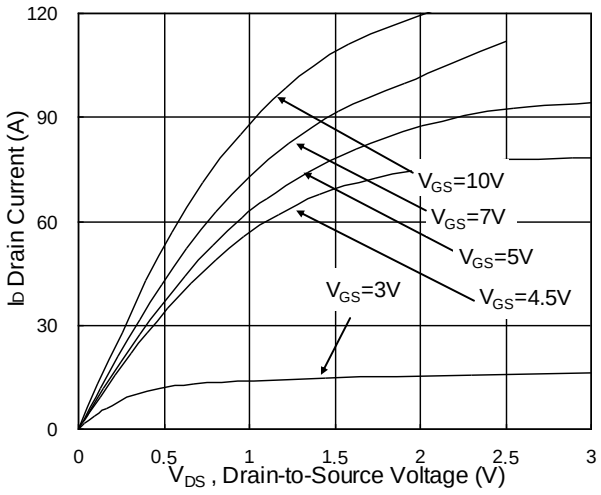



**Fig.1 Typical Output Characteristics**

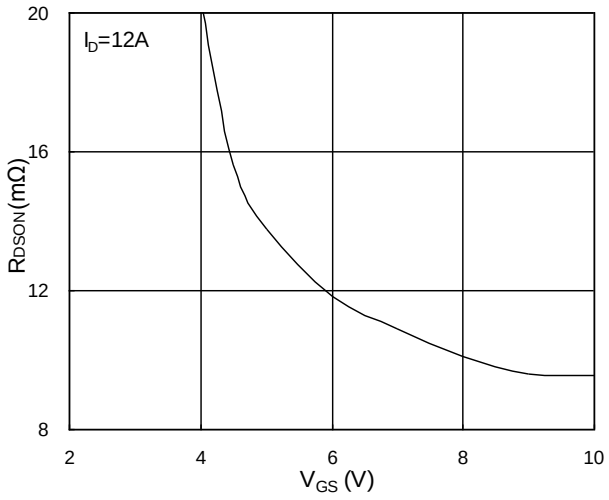



**Fig.2 On-Resistance vs. G-S Voltage**

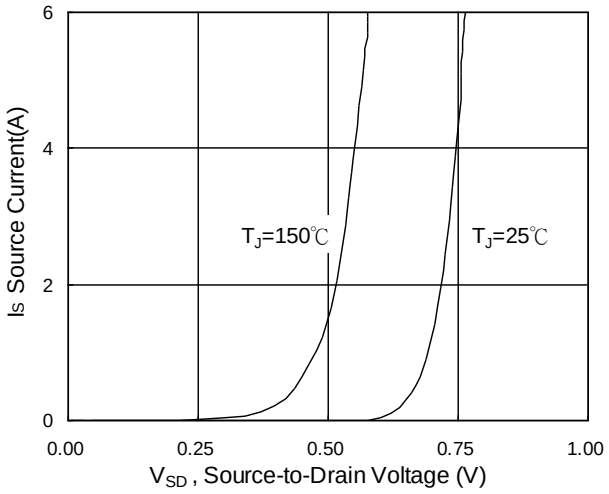



**Fig.3 Forward Characteristics of Reverse**

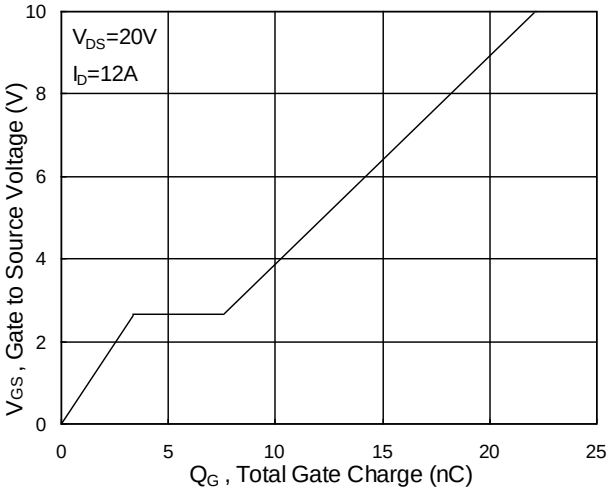



**Fig.4 Gate-Charge Characteristics**

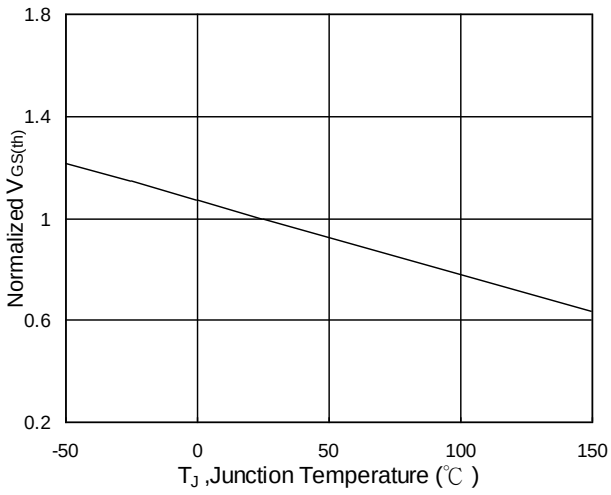



**Fig.5 $V_{GS(th)}$ vs. $T_J$**

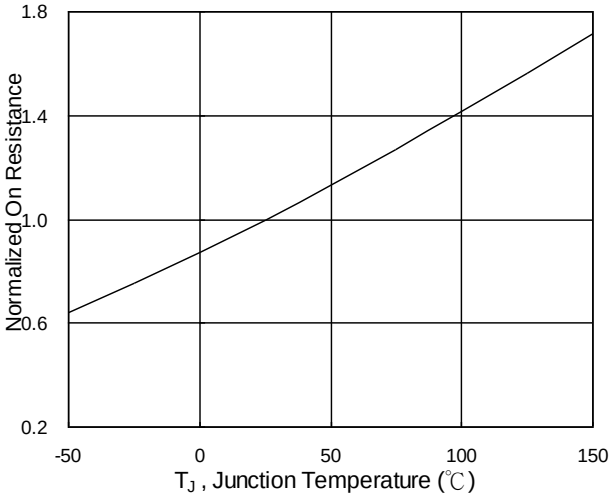



**Fig.6 Normalized $R_{DSON}$ vs. $T_J$**

## 40V N-Channel Enhancement Mode MOSFET

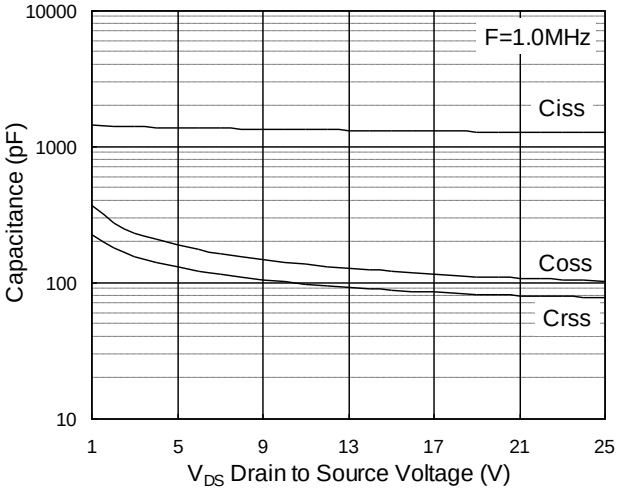



**Fig.7 Capacitance**

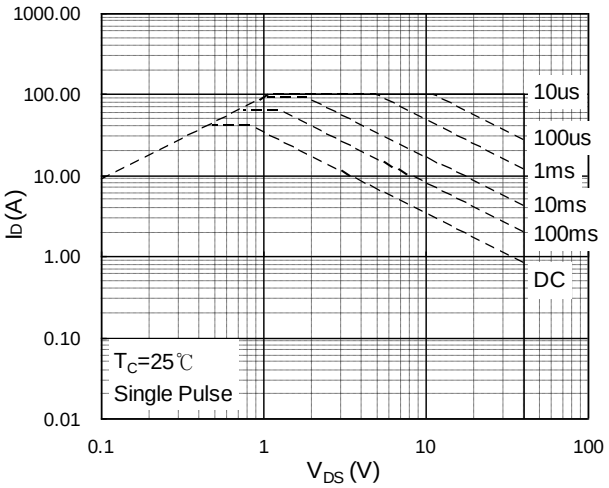



**Fig.8 Safe Operating Area**

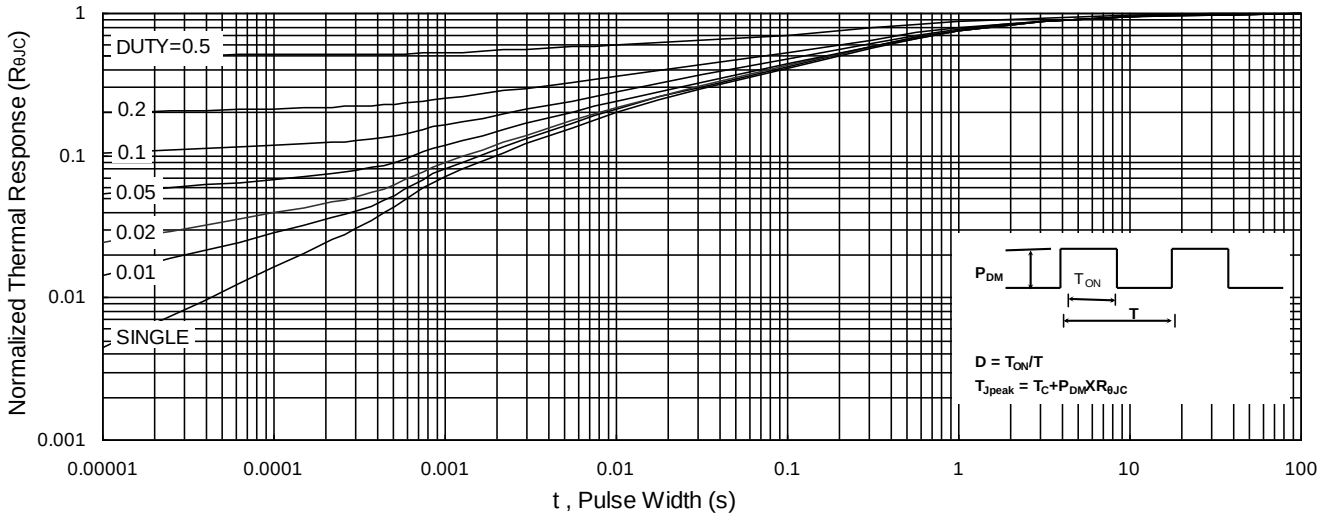



**Fig.9 Normalized Maximum Transient Thermal Impedance**

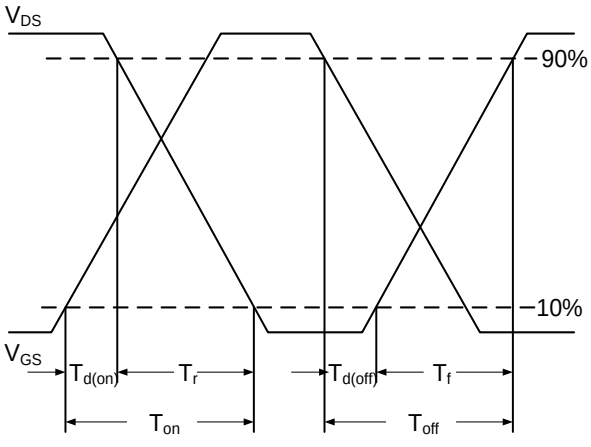



**Fig.10 Switching Time Waveform**

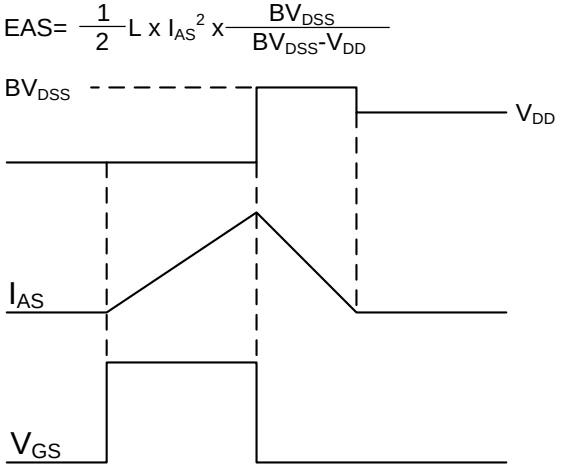
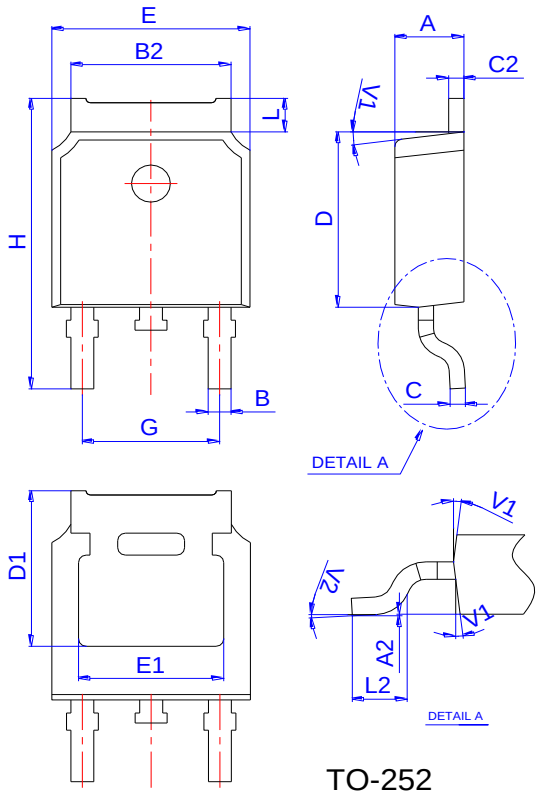



**Fig.11 Unclamped Inductive Switching Waveform**

## 40V N-Channel Enhancement Mode MOSFET

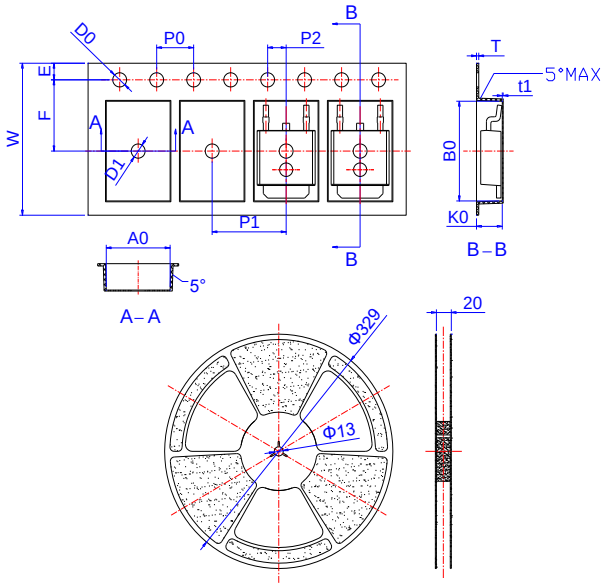
## Package Mechanical Data




TO-252

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 2.10 | | 2.50 | 0.083 | | 0.098 |
| A2 | 0 | | 0.10 | 0 | | 0.004 |
| B | 0.66 | | 0.86 | 0.026 | | 0.034 |
| B2 | 5.18 | | 5.48 | 0.202 | | 0.216 |
| C | 0.40 | | 0.60 | 0.016 | | 0.024 |
| C2 | 0.44 | | 0.58 | 0.017 | | 0.023 |
| D | 5.90 | | 6.30 | 0.232 | | 0.248 |
| D1 | 5.30REF | | | 0.209REF | | |
| E | 6.40 | | 6.80 | 0.252 | | 0.268 |
| E1 | 4.63 | | | 0.182 | | |
| G | 4.47 | | 4.67 | 0.176 | | 0.184 |
| H | 9.50 | | 10.70 | 0.374 | | 0.421 |
| L | 1.09 | | 1.21 | 0.043 | | 0.048 |
| L2 | 1.35 | | 1.65 | 0.053 | | 0.065 |
| V1 | | 7° | | | 7° | |
| V2 | 0° | | 6° | 0° | | 6° |

## Reel Specification-TO-252




| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| W | 15.90 | 16.00 | 16.10 | 0.626 | 0.630 | 0.634 |
| E | 1.65 | 1.75 | 1.85 | 0.065 | 0.069 | 0.073 |
| F | 7.40 | 7.50 | 7.60 | 0.291 | 0.295 | 0.299 |
| D0 | 1.40 | 1.50 | 1.60 | 0.055 | 0.059 | 0.063 |
| D1 | 1.40 | 1.50 | 1.60 | 0.055 | 0.059 | 0.063 |
| P0 | 3.90 | 4.00 | 4.10 | 0.154 | 0.157 | 0.161 |
| P1 | 7.90 | 8.00 | 8.10 | 0.311 | 0.315 | 0.319 |
| P2 | 1.90 | 2.00 | 2.10 | 0.075 | 0.079 | 0.083 |
| A0 | 6.85 | 6.90 | 7.00 | 0.270 | 0.271 | 0.276 |
| B0 | 10.45 | 10.50 | 10.60 | 0.411 | 0.413 | 0.417 |
| K0 | 2.68 | 2.78 | 2.88 | 0.105 | 0.109 | 0.113 |
| T | 0.24 | | 0.27 | 0.009 | | 0.011 |
| t1 | 0.10 | | | 0.004 | | |
| 10P0 | 39.80 | 40.00 | 40.20 | 1.567 | 1.575 | 1.583 |

Flow (wave) soldering (solder dipping)

| Product | Peak Temperature | Dipping Time |
|---|---|---|
| Pb device | 245℃±5℃ | 5sec±1sec |
| Pb-Free device | 260℃+0/-5℃ | 5sec±1sec |

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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