-30V P-Channel Enhancement Mode MOSFET

RoHS COMPLIANT

Description

The XPX4435XS uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a load switch or in PWM applications.

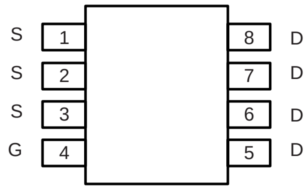
V_{DS} =-30V,I_D =-10.5A

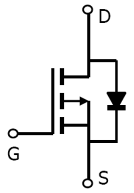
$R_{DS(ON)}$=12mΩ (typ) @ V_{GS}=10V

$R_{DS(ON)}$=18mΩ (typ) @ V_{GS}=4.5V

General Features

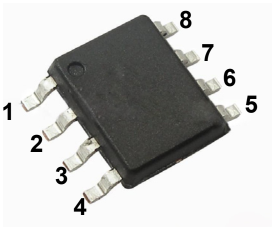
- High Power and current handing capability
- Lead free product is acquired
- Surface mount package





Application

- PWM applications
- Load switch
- Power management



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
XPX4435XS	SOP-8	XPX4435XS XXX YYYY	3000

Absolute Maximum Ratings (TC=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	-30	V
VGS	Gate-Source Voltage	±20	V
I_D@T_A=25℃	Continuous Drain Current, V_{GS} @ -10V[1]	-10.5	A
I_D@T_A=70℃	Continuous Drain Current, V_{GS} @ -10V[1]	-8.6	A
IDM	Pulsed Drain Current[2]	-50	A
EAS	Single Pulse Avalanche Energy[3]	72.2	mJ
IAS	Avalanche Current	-38	A
P_D@T_A=25℃	Total Power Dissipation[4]	3.1	W
P_D@T_A=70℃	Total Power Dissipation[4]	2	W
TSTG	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
$R_{\theta}JA$	Thermal Resistance Junction-Ambient [1]	75	℃/W
$R_{\theta}JA$	Thermal Resistance Junction-Ambient [1](t≦ 10s)	40	℃/W
$R_{\theta}JC$	Thermal Resistance Junction-Case[1]	24	℃/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-30	-32	---	V
△BVDSS/△TJ	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.022	---	V/℃
RDS(ON)	Static Drain-Source On-Resistance[2]	V_{GS}=-10V , I_D=-10A	---	12	16	mΩ
		V_{GS}=-4.5V , I_D=-5A	---	18	24	
VGS(th)	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-1.0	-1.6	-2.5	V
△$V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.6	---	mV/℃
IDSS	Drain-Source Leakage Current	V_{DS}=-24V , V_{GS}=0V , T_J=25℃	---	---	-1	uA
		V_{DS}=-24V , V_{GS}=0V , T_J=55℃	---	---	-5	
IGSS	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-5A	---	17	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	13	---	Ω
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-15V , V_{GS}=-4.5V , I_D=-6A	---	30	---	nC
Qgs	Gate-Source Charge		---	6	---	
Qgd	Gate-Drain Charge		---	9	---	
Td(on)	Turn-On Delay Time	V_{DD}=-15V , V_{GS}=-10V , R_G=3.3Ω, I_D=-6A	---	10	---	ns
T_r	Rise Time		---	26	---	
Td(off)	Turn-Off Delay Time		---	35	---	
T_f	Fall Time		---	8	---	
Ciss	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , f=1MHz	---	1800	---	pF
Coss	Output Capacitance		---	305	---	
Crss	Reverse Transfer Capacitance		---	216	---	
IS	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	---	---	-10	A
ISM	Pulsed Source Current[2,5]		---	---	-50	A
VSD	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1.2	V
trr	Reverse Recovery Time	IF=-6A , dI/dt=100A/μs , T_J=25℃	---	16.3	---	nS
Q_{rr}	Reverse Recovery Charge		---	5.9	---	nC

Note :

1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3、The EAS data shows Max. rating . The test condition is VDD=-25V,VGS=-10V,L=0.1mH,IAS=-38A
4、The power dissipation is limited by 150℃ junction temperature
5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

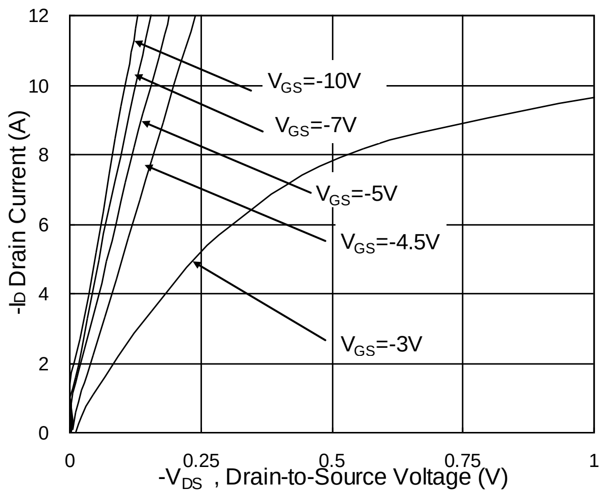


Fig.1 Typical Output Characteristics

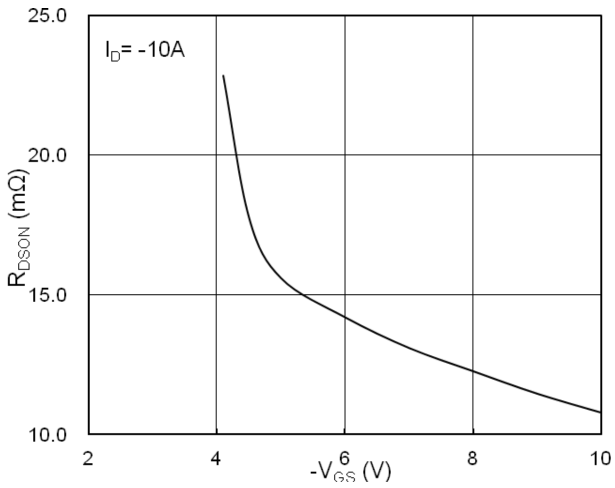


Fig.2 On-Resistance vs. G-S Voltage

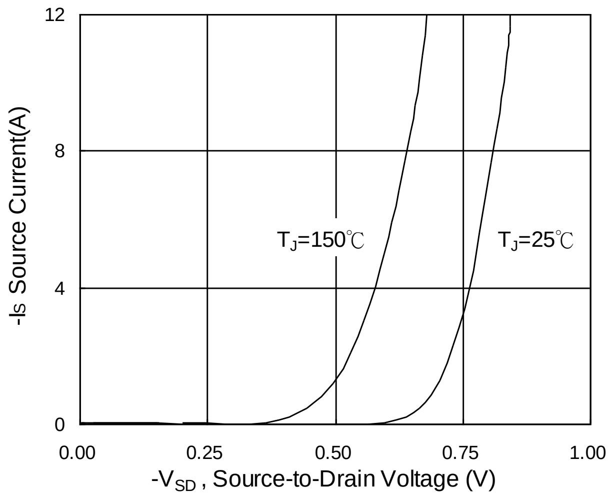


Fig.3 Forward Characteristics of Reverse

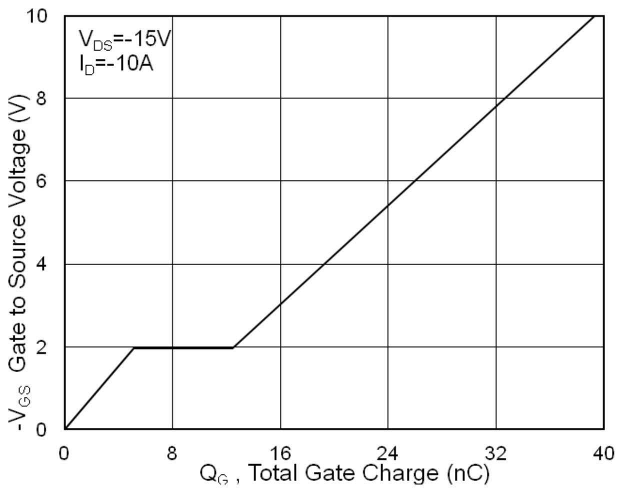


Fig.4 Gate-charge Characteristics

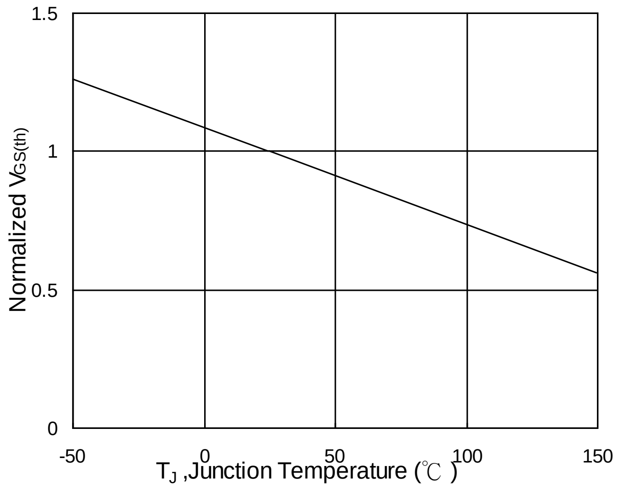


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

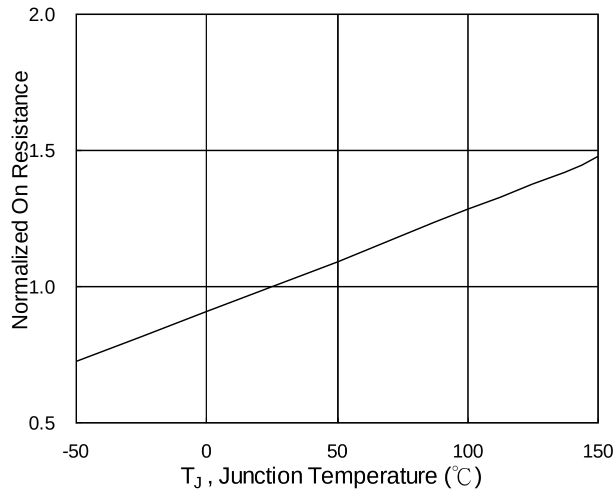


Fig.6 Normalized R_{DSON} vs. T_J

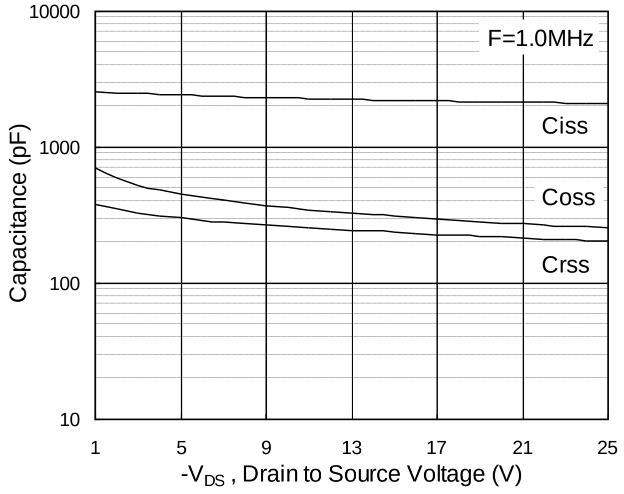


Fig.7 Capacitance

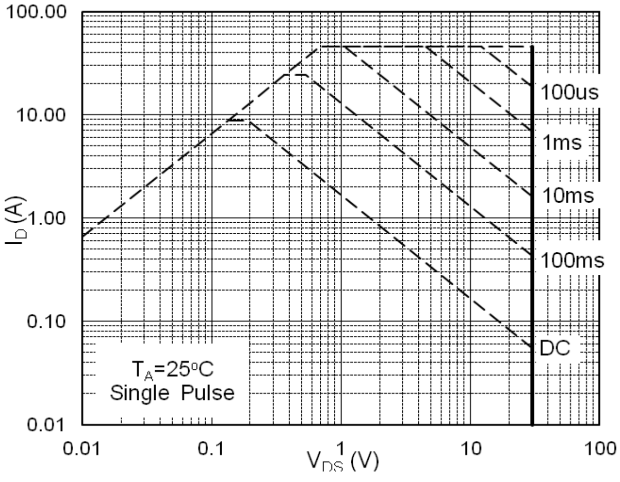


Fig.8 Safe Operating Area

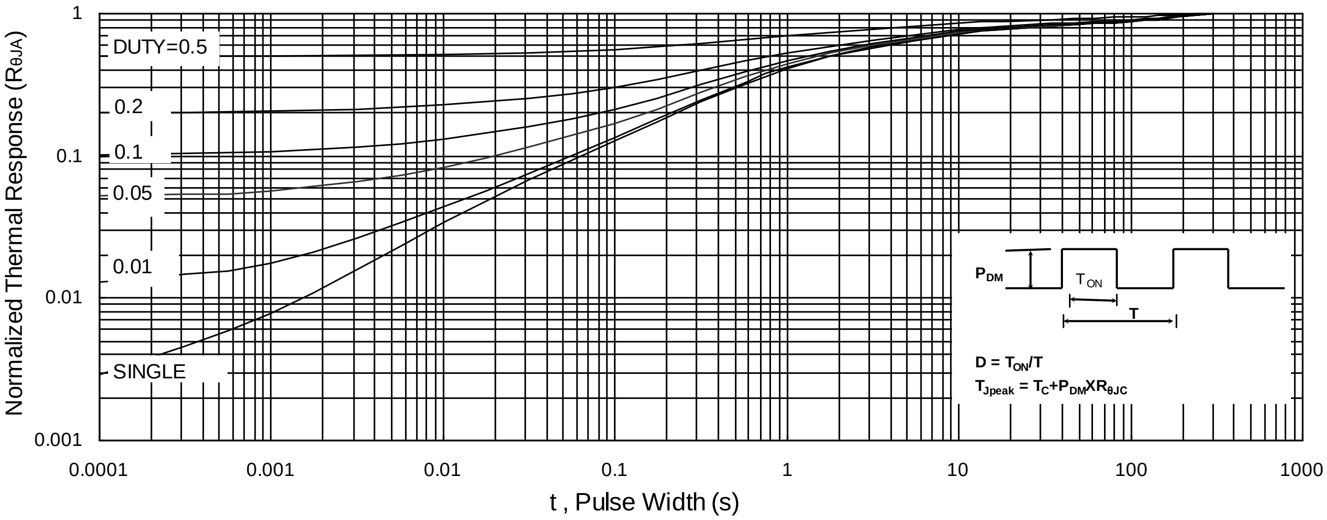


Fig.9 Normalized Maximum Transient Thermal Impedance

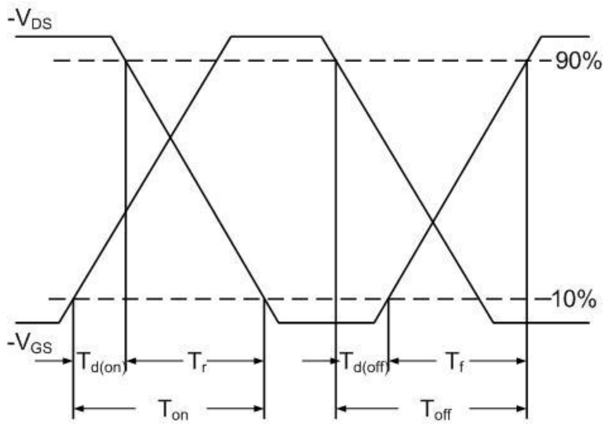


Fig.10 Switching Time Waveform

$$EAS=\frac{1}{2}L\times(-I_{AS}^{2})\times\frac{-BV_{DSS}}{-BV_{DSS}-(-V_{DD})}$$

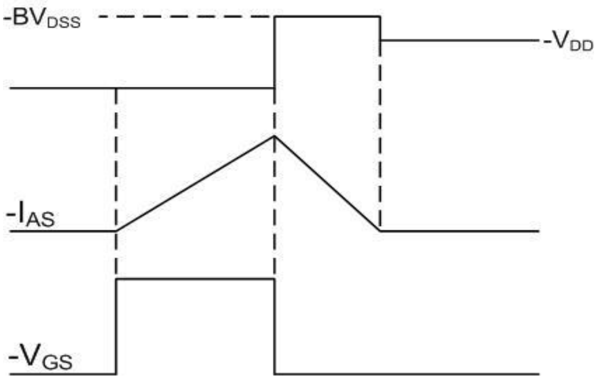
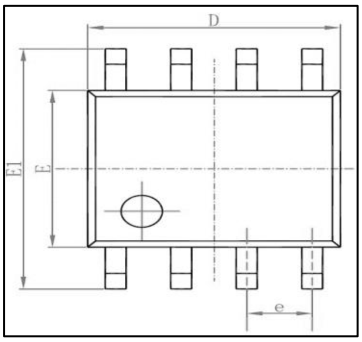
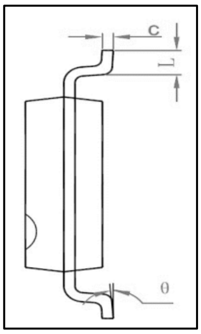
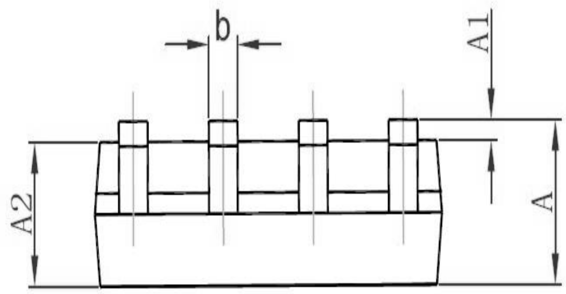


Fig.11 Unclamped Inductive Waveform

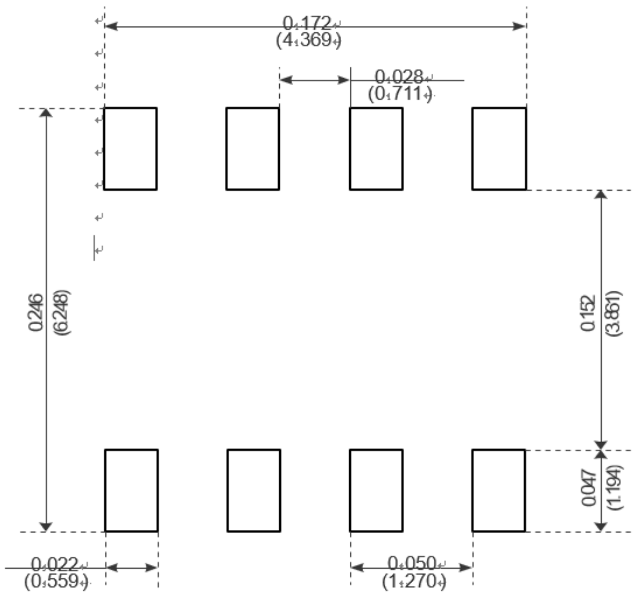
Package Mechanical Data-SOP-8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1. 350	1. 750	0. 053	0. 069
A1	0. 100	0. 250	0. 004	0. 010
A2	1. 350	1. 550	0. 053	0. 061
b	0. 330	0. 510	0. 013	0. 020
c	0. 170	0. 250	0. 006	0. 010
D	4. 700	5. 100	0. 185	0. 200
E	3. 800	4. 000	0. 150	0. 157
E1	5. 800	6. 200	0. 228	0. 244
e	1. 270 (BSC)		0. 050 (BSC)	
L	0. 400	1. 270	0. 016	0. 050
θ	0°	8°	0°	8°



Recommended Minimum Pads

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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