


Description

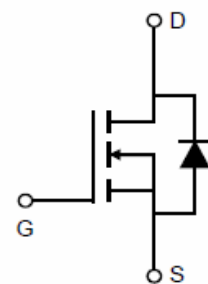
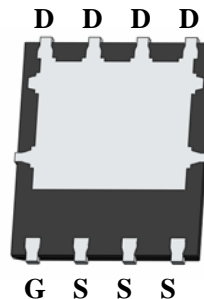
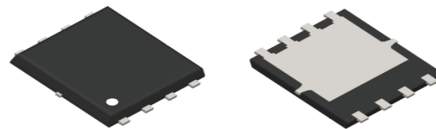
The XPX2N2U8RD uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

 $V_{DS} = 20V, I_D = 80A$
 $R_{DS(ON)} = 2.8m\Omega$ (typ) @ $V_{GS} = 4.5V$
 $R_{DS(ON)} = 4.0m\Omega$ (typ) @ $V_{GS} = 2.5V$
Application

solar road lights

Load switch

Uninterruptible power supply


Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
XPX2N2U8RD	PDFN5*6-8L	XPX2N2U8RD XXX YYYY	5000

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Max.	Units
V_{DSS}	Drain-Source Voltage	20	V
V_{GSS}	Gate-Source Voltage	± 12	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	80	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	59	A
IDM	Pulsed Drain Current ^{note1}	360	A
EAS	Single Pulsed Avalanche Energy ^{note2}	110	mJ
P_D	Power Dissipation	81	W
$R_{\theta JA}$	Thermal Resistance, Junction to Case	65	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case 1	4	$^\circ C/W$
TJ, TSTG	Operating and Storage Temperature Range	-55 to +175	$^\circ C$

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BVDSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	20	24		V
ΔBVDSS/ΔTJ	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.018	---	V/°C
VGS(th)	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	0.50	0.65	1.0	V
RDS(ON)	Static Drain-Source On-Resistance	V _{GS} =4.5V, I _D =30A		2.8	4.0	mΩ
RDS(ON)	Static Drain-Source On-Resistance	V _{GS} =2.5V, I _D =20A		4.0	6.0	
IDSS	Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0V			1	μA
IGSS	Gate-Body Leakage Current	V _{GS} =±10V, V _{DS} =0V			±100	nA
C _{iss}	Input Capacitance	V _{DS} =10V, V _{GS} =0V, f=1MHZ		3200		pF
C _{oss}	Output Capacitance			460		
C _{rss}	Reverse Transfer Capacitance			446		
Q _g	Total Gate Charge	V _{GS} =4.5V, V _{DS} =10V, I _D =30A		11.05		nC
Q _{gs}	Gate-Source Charge			1.73		
Q _{gd}	Gate-Drain Charge			3.1		
tD(on)	Turn-on Delay Time	V _{GS} =4.5V, V _{DS} =10V, I _D =30A R _{GEN} =1.8Ω		9.7		ns
t _r	Turn-on Rise Time			37		
tD(off)	Turn-off Delay Time			63		
t _f	Turn-off fall Time			52		
V _{SD}	Diode Forward Voltage	I _S =7.6A, V _{GS} =0V			1.2	V

Note :

- 1、 The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≅ 300us , duty cycle ≅ 2%
- 3、 The power dissipation is limited by 150°C junction temperature
- 4、 The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.
- 5、 EAS condition: T_J=25°C, V_{DD}=15V, V_G=4.5V, R_G=25Ω, L=0.5mH, I_{AS}=21A

Typical Characteristics

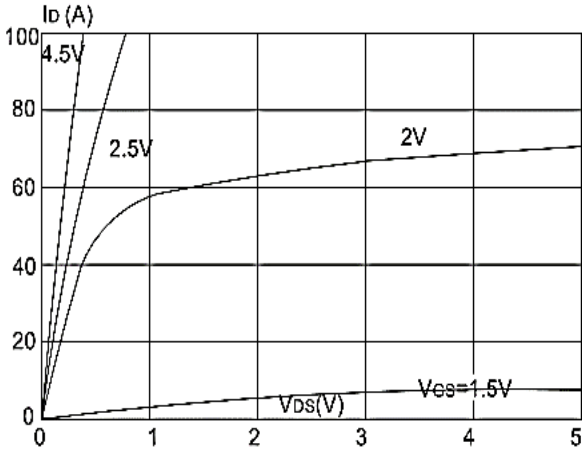


Figure 1: Output Characteristics

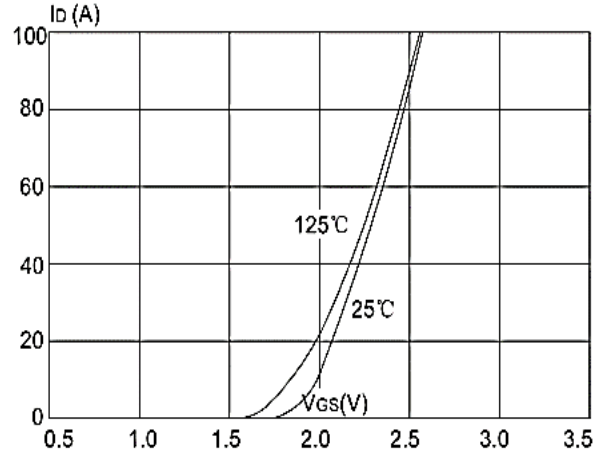


Figure 2: Typical Transfer Characteristics

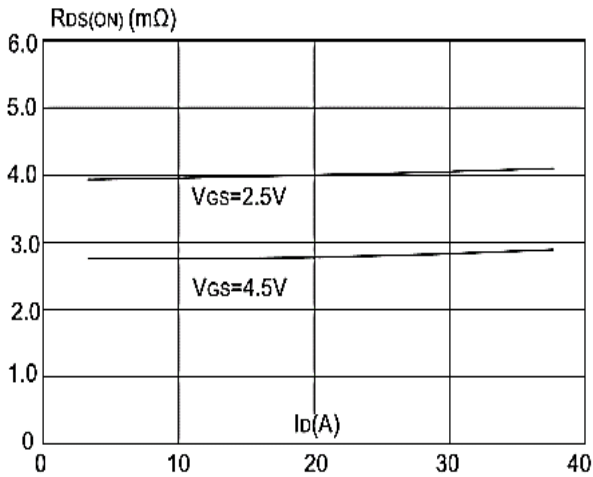


Figure 3: On-resistance vs. Drain Current

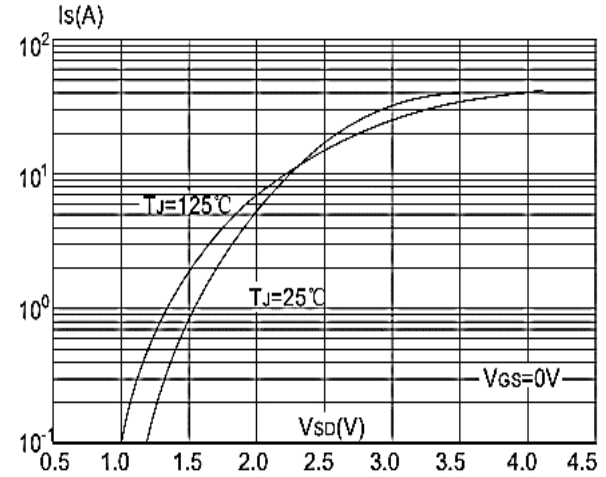


Figure 4: Body Diode Characteristics

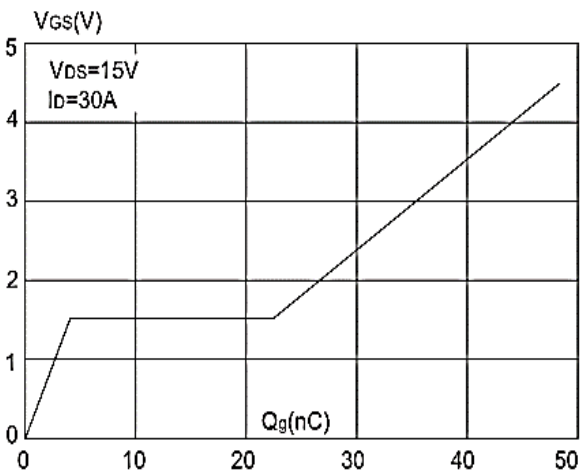


Figure 5: Gate Charge Characteristics

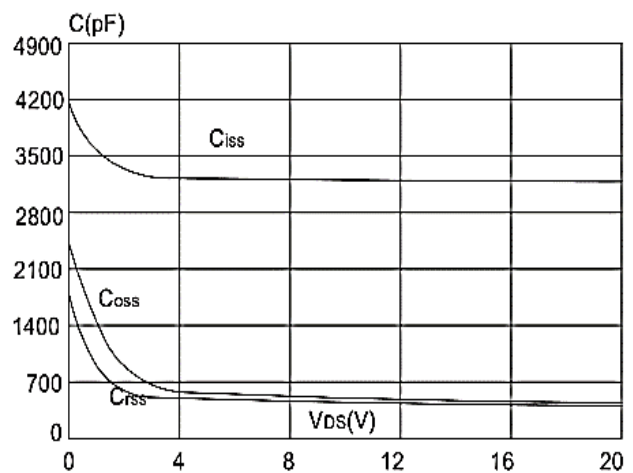


Figure 6: Capacitance Characteristics

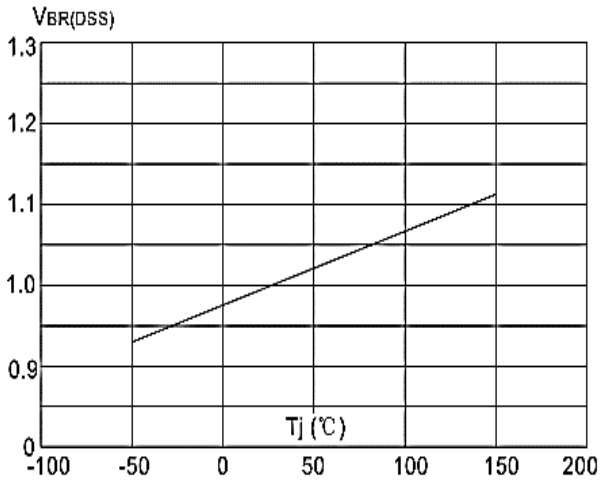


Figure 7: Normalized Breakdown Voltage vs Junction Temperature

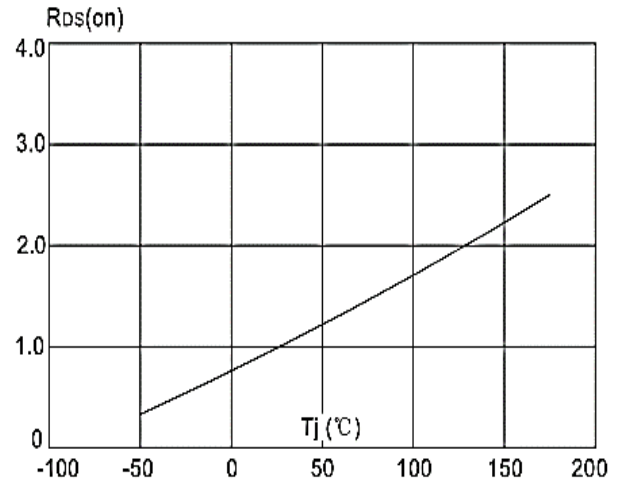


Figure 8: Normalized on Resistance vs. Junction Temperature

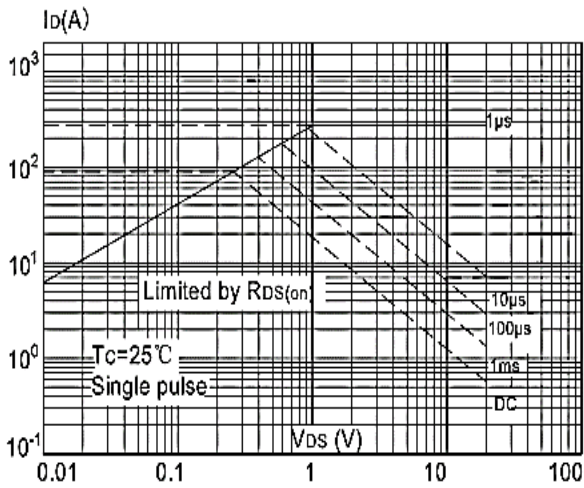


Figure 9: Maximum Safe Operating Area

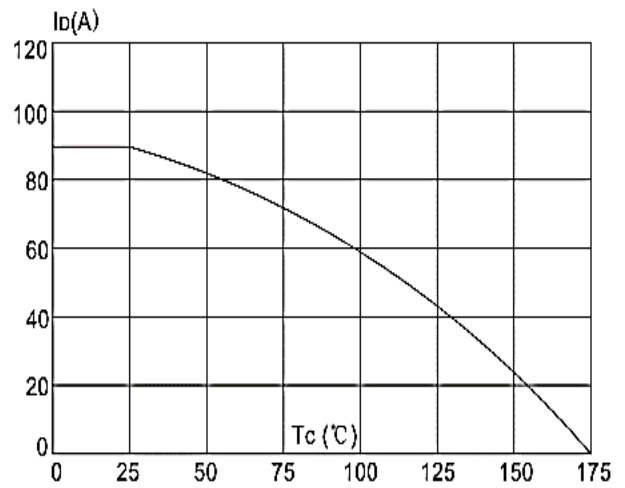


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

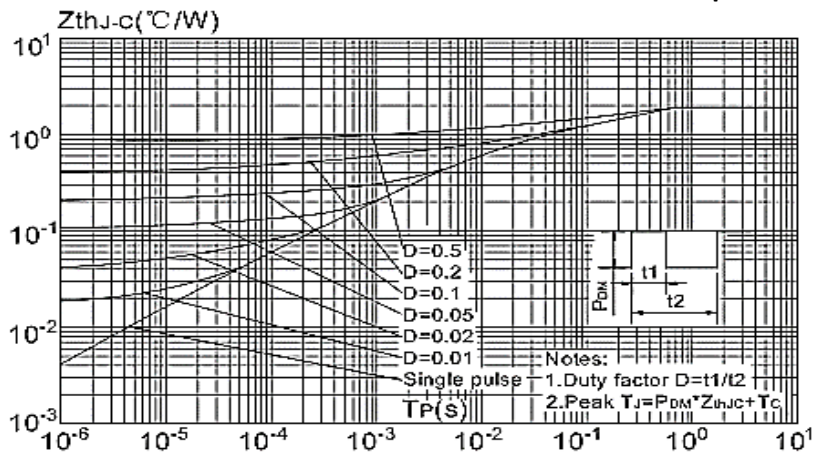
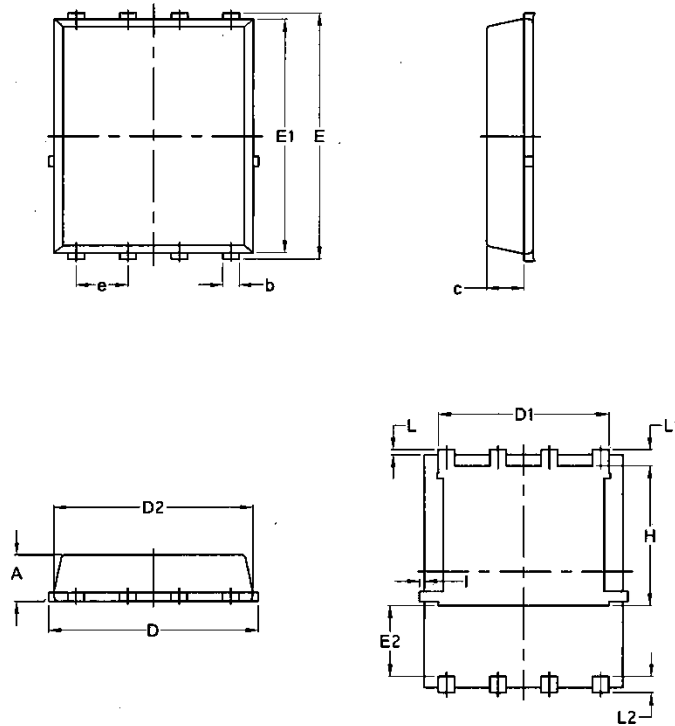


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambien

Package Mechanical Data-DFN5*6-8L-JQ Single


Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245°C ±5°C	5sec ±1 sec
Pb-Free device	260°C +0/-5°C	5sec ±1 sec



This integrated circuit can be damaged by ESD. UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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