XPX20L45RX

-20V P-Channe Enhancement Mode MOSFET

RoHS COMPLIANT

Description

The XPX20L45RX uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

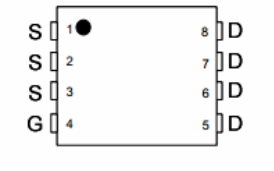
V_{DS} =-20V,I_D =-45A

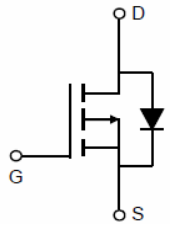
$R_{DS(ON)}$=12mΩ (typ) @ V_{GS}=-4.5V

$R_{DS(ON)}$=18mΩ (typ) @ V_{GS}=-2.5V

General Features

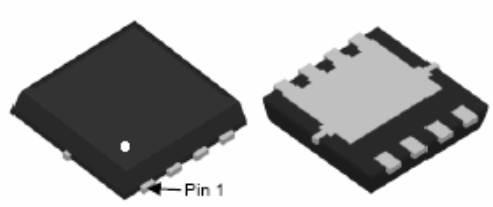
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation





Application

- Load switch
- Battery protection



DFN 3.3x3.3-8L

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
XPX20L45RX	XPX20L45RX	DFN 3.3x3.3-8L	-	-	5000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	±12	V
Drain Current-Continuous	I_D	-45	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	-35	A
Pulsed Drain Current	I_{DM}	-43	A
Maximum Power Dissipation	P_D	22	W
Single pulse avalanche energy (Note 5)	E_{AS}	38	mJ
Derating factor		0.55	W/℃
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃
Thermal Resistance,Junction-to-Case(Note 2)	$R_{\theta JC}$	2.6	℃/W

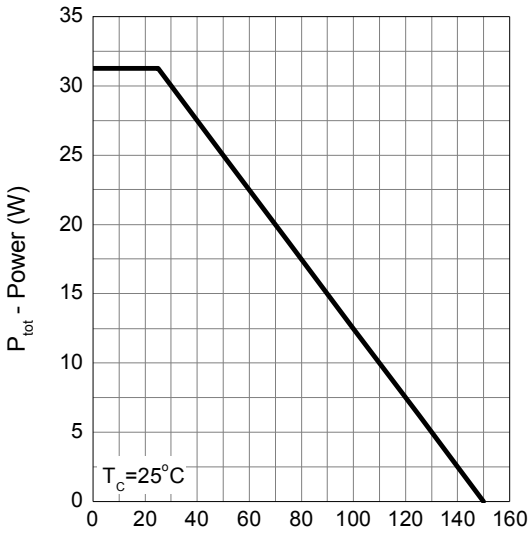
Electrical Characteristics (T_A = 25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=-250μA	-20	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-16V, V_{GS}=0V	-	-	-1	μA
		T_J=85°C	-	-	-30	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=-250μA	-0.5	-	-1	V
I_{GSS}	Gate Leakage Current	V_{GS}=±12V, V_{DS}=0V	-	-	±10	μA
$R_{DS(ON)}$ [e]	Drain-Source On-state Resistance	V_{GS}=-4.5V, I_{DS}=-11A	-	12	17	mΩ
		V_{GS}=-2.5V, I_{DS}=-6A	-	18	25	
		V_{GS}=-1.8V, I_{DS}=-1A	-	26	45	
Diode Characteristics						
V_{SD} [e]	Diode Forward Voltage	I_{SD}=-1A, V_{GS}=0V	-	-0.7	-1	V
t_{rr} [f]	Reverse Recovery Time	I_{SD}=-11A, dI_{SD}/dt=100A/μs	-	63	-	ns
Q_{rr} [f]	Reverse Recovery Charge		-	54	-	nC
Dynamic Characteristics [f]						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-10V, Frequency=1.0MHz	-	1620	-	pF
C_{oss}	Output Capacitance		-	320	-	
C_{rss}	Reverse Transfer Capacitance		-	290	-	
$t_{d(ON)}$	Turn-on Delay Time	V_{DD}=-10V, R_L=10Ω, I_{DS}=-1A, V_{GEN}=-4.5V, R_G=6Ω	-	9	-	ns
t_r	Turn-on Rise Time		-	13	-	
$t_{d(OFF)}$	Turn-off Delay Time		-	26	-	
t_f	Turn-off Fall Time		-	167	-	
Gate Charge Characteristics [f]						
Q_g	Total Gate Charge	V_{DS}=-10V, V_{GS}=-4.5V, I_{DS}=-11A	-	25	-	nC
Q_{gs}	Gate-Source Charge		-	1.6	-	
Q_{gd}	Gate-Drain Charge		-	11	-	

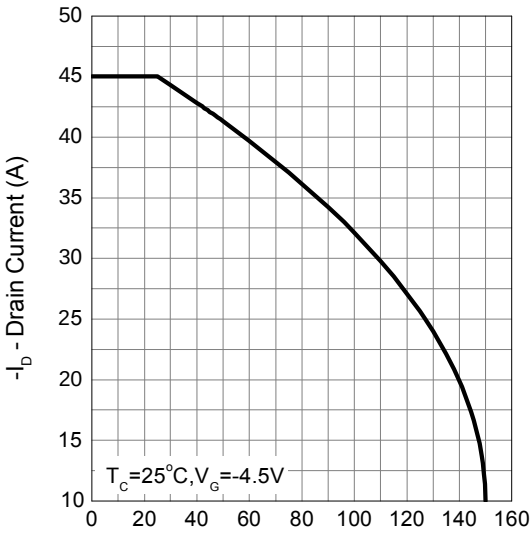
Note e：Pulse test; pulse width≤300μs, duty cycle≤2%.
Note f：Guaranteed by design, not subject to production testing.

Typical Operating Characteristics

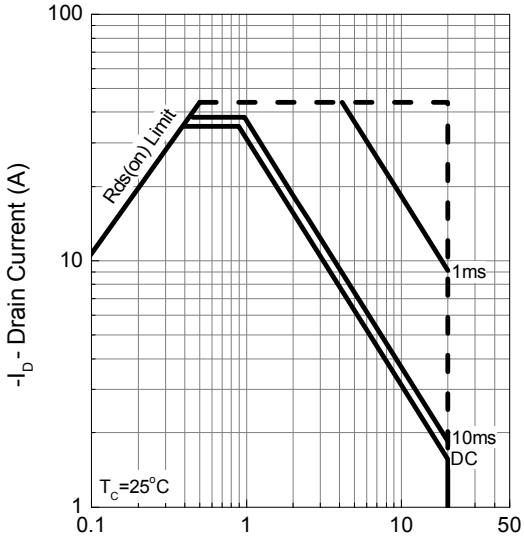
Power Dissipation



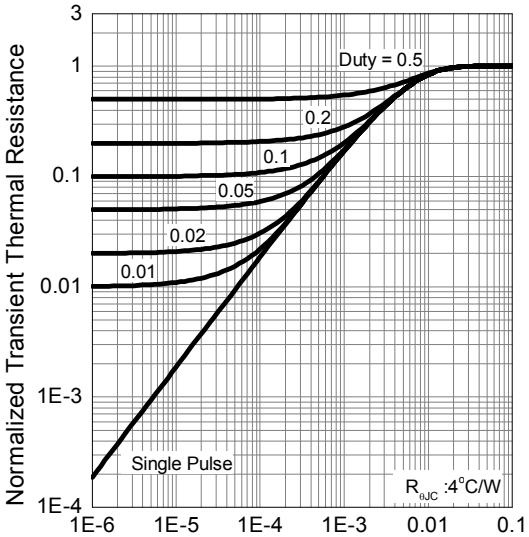
Drain Current



Safe Operation Area

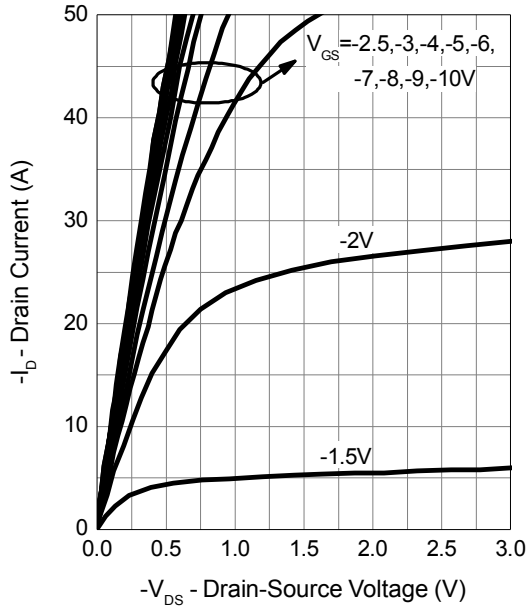


Thermal Transient Impedance

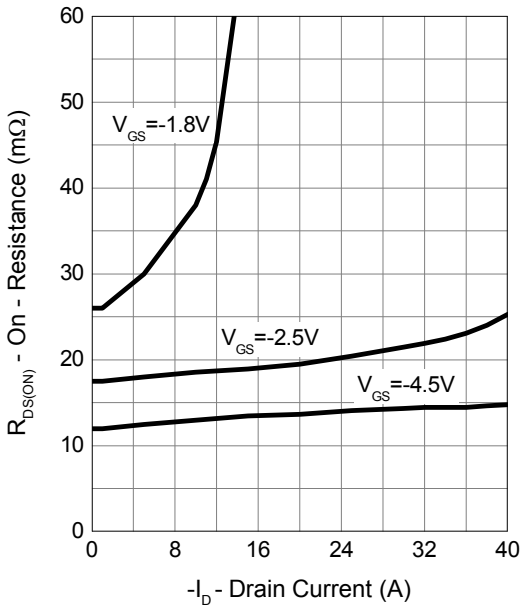


Typical Operating Characteristics (Cont.)

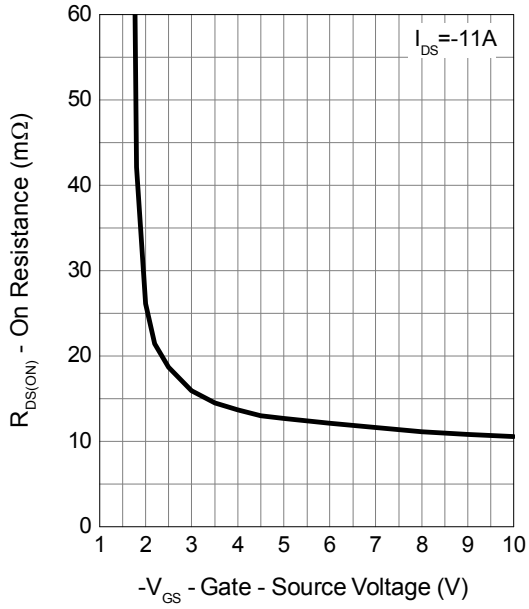
Output Characteristics



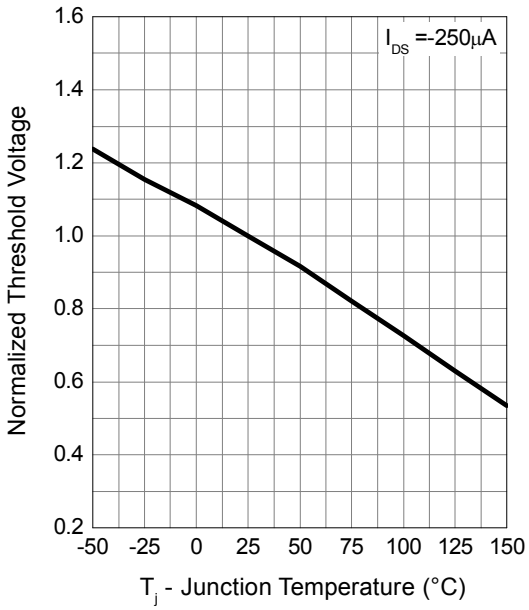
Drain-Source On Resistance



Gate-Source On Resistance

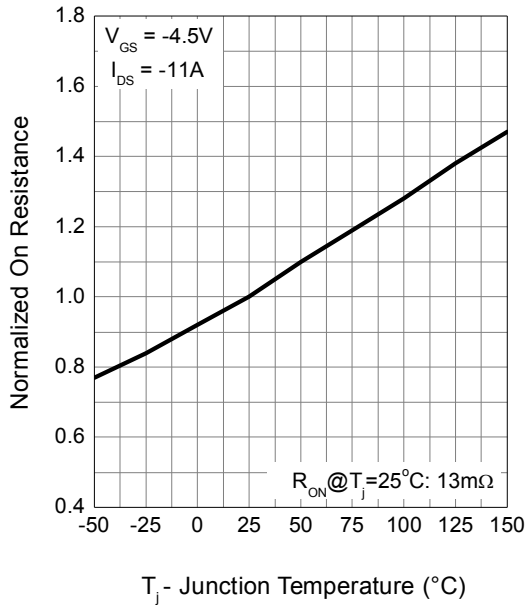


Gate Threshold Voltage

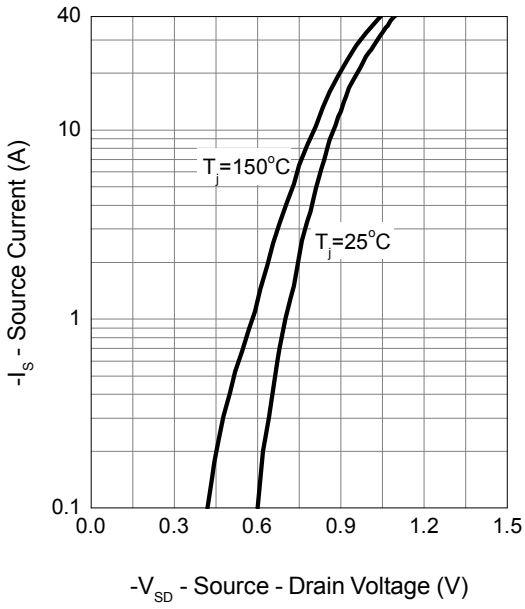


Typical Operating Characteristics (Cont.)

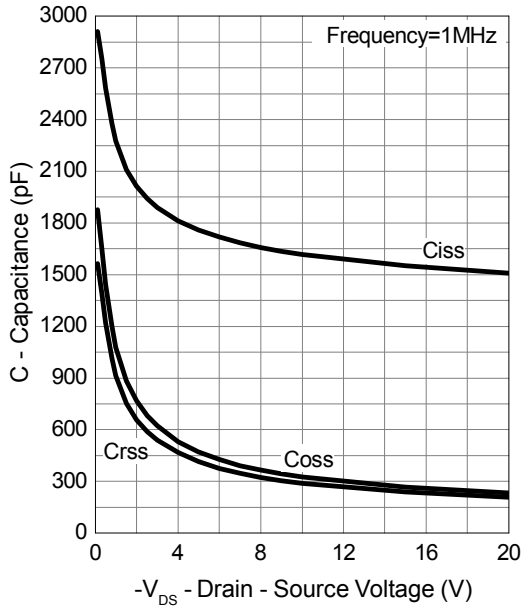
Drain-Source On Resistance



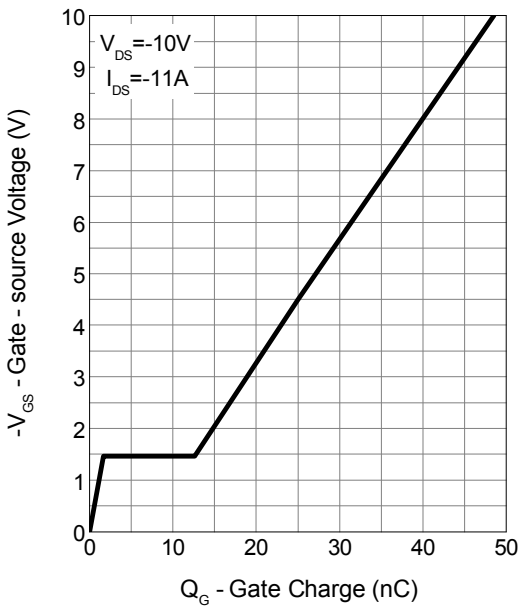
Source-Drain Diode Forward



Capacitance

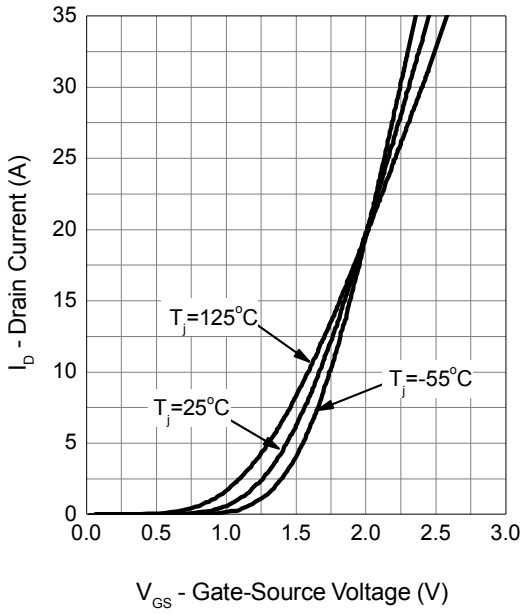


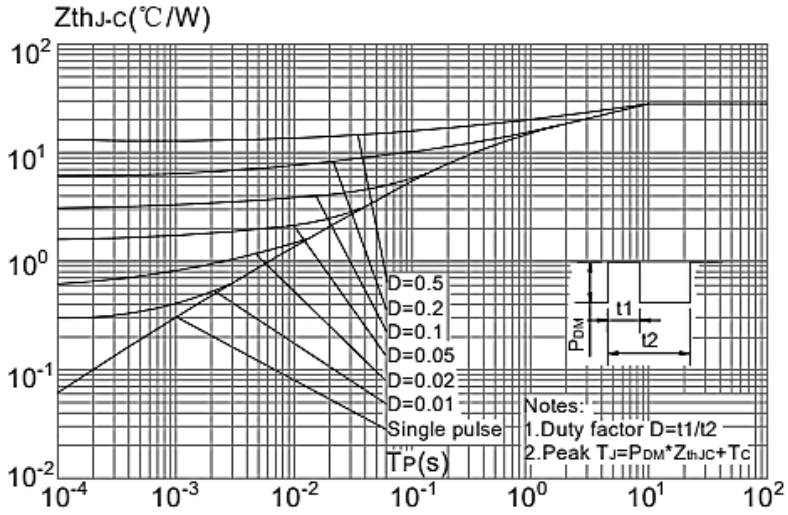
Gate Charge



Typical Operating Characteristics (Cont.)

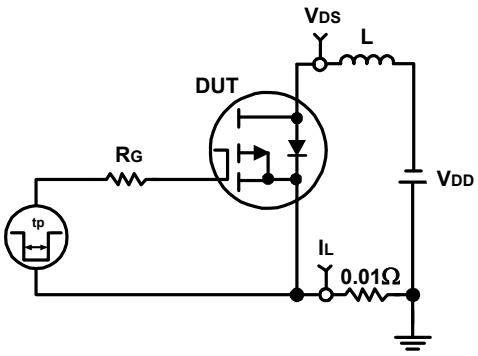
Transfer Characteristics

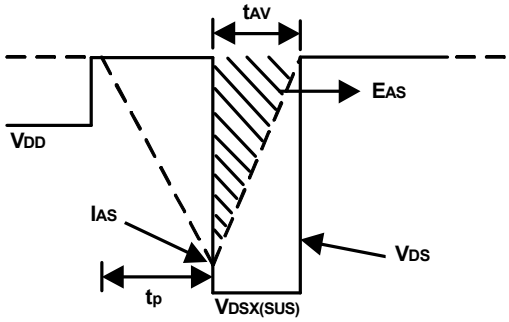




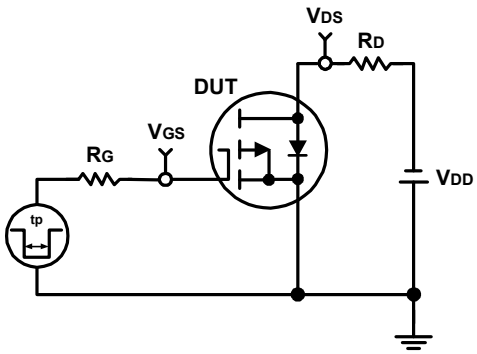
Maximum Effective Transient Thermal Impedance, Junction-to-Ambien

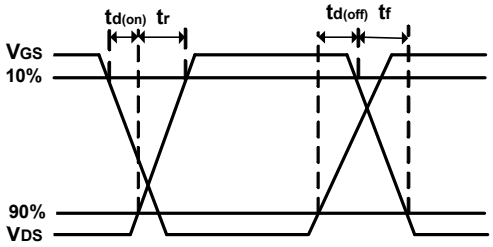
Avalanche Test Circuit and Waveforms





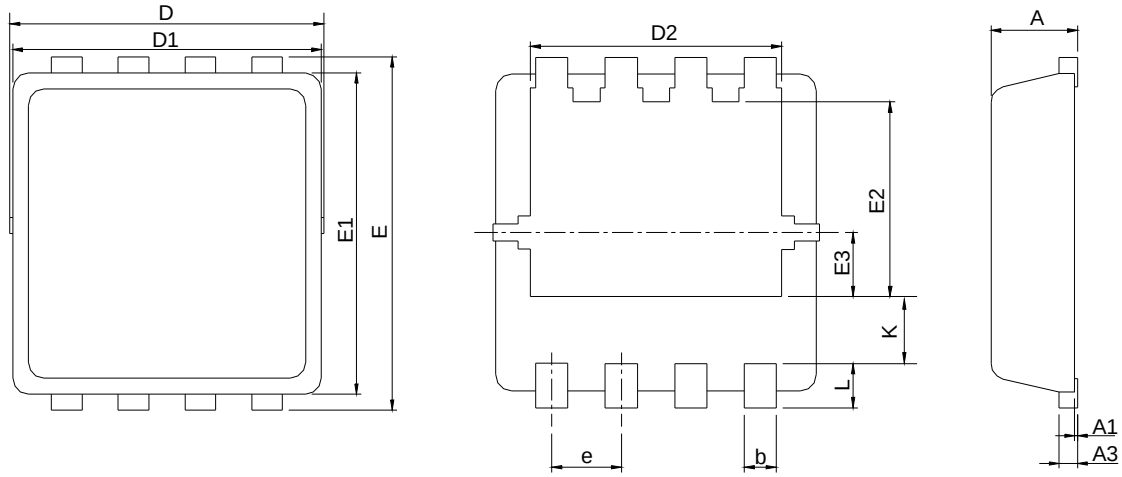
Switching Time Test Circuit and Waveforms





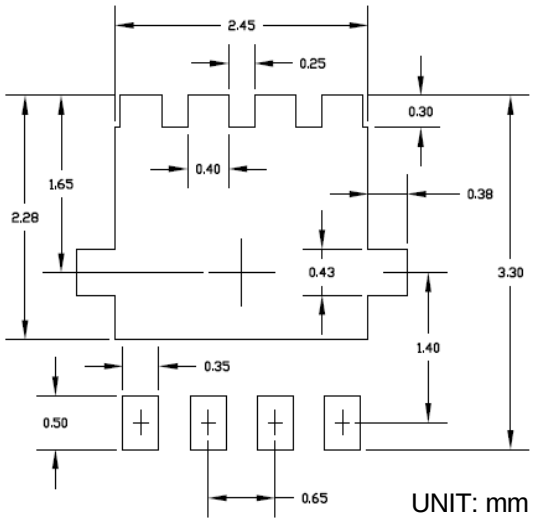
Package Information

DFN3.3x3.3-8L_EP1_P



SYMBOL	DFN3x3-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.10	0.25	0.004	0.010
b	0.24	0.35	0.009	0.014
D	2.90	3.30	0.114	0.130
D1	2.90	3.10	0.114	0.122
D2	2.25	2.45	0.089	0.096
E	3.10	3.30	0.122	0.130
E1	2.90	3.10	0.114	0.122
E2	1.65	1.85	0.065	0.073
E3	0.56	0.58	0.022	0.023
e	0.65 BSC		0.026 BSC	
K	0.475	0.775	0.019	0.031
L	0.30	0.50	0.012	0.020

RECOMMENDED LAND PATTERN



Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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